HIGH DENSITY MICROWAVE PACKAGING PROGRAM

Eliot D. Cohen

Advanced Research Projects Agency
Arlington, VA

INTRODUCTION

The objective of the High Density Microwave Packaging (HDMP) program is to develop and establish the producibility of complex shape, light weight, and high density microwave frequency transmit/receive (T/R) modules. The approach is to focus development on modules for active array radar applications, particularly for such platforms as the next-generation of F-22s, comparable Navy aircraft, and Army helicopters. A key technical requirement for successful fielding of active aperture phased arrays on aircraft and space-based platforms is to integrate all array elements, including radiating elements, microwave components, RF and DC interconnects, distribution channels, signal processing control elements, and thermal management systems into compact, minimum size packages that meet functional and environmental requirements. The entire assembly must lend itself to efficient and reproducible manufacture. Major program goals are: 1) reducing T/R module cost by an order of magnitude or more at required performance levels while achieving size, weight and form factor requirements; 2) making expanded use of coordinated microwave computer aided design (CAD), manufacturing (CAM), and test (CAT) capabilities for higher yields; 3) incorporating advanced technologies to meet performance, cost, weight and size requirements more effectively; and 4) meeting system requirements for T/R module reliability and hermeticity by using novel advanced microwave packaging techniques. This paper will discuss the program's structure and summarize the technical approaches being taken by the participating contractors to meet the program's goals.

PROGRAM STRUCTURE

The HDMP program is ARPA sponsored and ARPA/tri-Service managed. The Air Force's Wright Laboratory, the Army Research Laboratory-Fort Monmouth, Naval Air Systems Command, and the Naval Research Laboratory all participate in program management. The program is divided into two parts. The first part is directed toward the design and demonstration of highly integrated, advanced modules for microwave phased array radars. This portion of the program will culminate in demonstration of several approaches for providing the required modules and demonstration of an active phased array subsystem brassboard. Three contracts have been awarded to teams headed by Hughes Aircraft Co., Texas Instruments, and Westinghouse. The second part of the program is focused upon continuing advancements in related technology and computer aided design capabilities. The activities being undertaken in this portion of the program include: 1) Coatings for GaAs circuits which provide moisture and particle protection without significantly compromising RF performance; 2) Material characterization and database development; and 3) Advanced computer aided design, modeling, simulation and analysis tools.

TECHNICAL APPROACHES

The contractor teams participating in the first part of the program are pursuing the development of groups of T/R modules for use within the airborne radar frequency band extending from approximately 7 GHz to 11 GHz. These groups of modules are sometimes referred to as multi-chip assemblies

(MCAs) because they typically consist of sub-arrays of modules fabricated simultaneously and housed within a single package. At present, all of the HDMP contractors are developing 2x2 MCAs. As with all production methods used to form highly integrated assemblies, re-work, to repair defective parts, is very difficult and in some cases impossible. Consequently, there is a very high priority placed on assuring that all microwave monolithic integrated circuits (MMICs) and other parts used in these MCAs perform in a known and predictable manner, prior to their use in assemblies (i.e., known good die (KGD) are necessary). Current MMIC manufacturing and KGD yields only support the production of relatively small (2x2) sub-arrays, but as MMIC production and KGD yields improve, MCA assemblies will be extended to 4x4 and 6x6 configurations.

The types of modules being developed are sometimes called "tiles" because of their approximately cubic dimensions as opposed to the older, more conventional "brick" style T/R modules which, in general, include all circuitry on one plane and have a long thin appearance. The tile modules consist of multiple interconnection layers with MMICs and other components mounted on their top surface (nearest the antenna). In one architectural approach, high power amplifiers are placed on the top of one set of interconnection layers, other microwave components on the top of a second set, and control components (including silicon digital integrated circuits) on top of a third. The three sets of layers are then batch interconnected with each other to form a complete multi-channel MCA. Other approaches group the microwave components in one set and dc or low frequency control components in another. Either of these types of module architectures lend themselves to batch fabrication and assembly and make it easy to fabricate sub-arrays of T/R modules simultaneously, thus, saving substantially on the cost of both manufacture and assembly. The use of a tile approach enhances the likelihood of achieving the long sought after goal of T/R module unit cost of less than $200 per channel.

Although all of the HDMP primary phase contractors are working toward the development of tile architecture modules, each is using a different approach. Hughes Aircraft Company is using multi-layer tiles fabricated from aluminum nitride to form 2x2 module arrays. Aluminum nitride was selected because of its superior thermal properties, low cost, and its coefficient of thermal expansion (CTE), which is a good match to that of both silicon and gallium arsenide. The first layer of the array, called the common leg circuit or CLC tile, is a 16 layer assembly containing a variable gain amplifier, phase shifter, switches, and a separate silicon microprocessor chip for control of each of the four modules. The second layer, the Driver/LNA tile, is a six layer structure, containing four transmit driver amplifier MMICs and four receiver low noise amplifier MMICs. The final or top layer is a ten layer structure which contains four high power MMIC amplifier chips each yielding a nominal output power of approximately 8 watts. The entire assembly is approximately 1 inch square and 0.25 inch thick. All of the integrated circuits used, both MMICs and silicon, are mounted in a "flip-chip" position. This eliminates a large number of wire-bond interconnects while providing effective heat removal paths. Sixteen 2x2 arrays, providing sixty-four T/R channels, have been fabricated for Hughes by Coors and are in the process of being tested.

Although the technical approach being taken by Hughes, as well as those of other companies participating in the HDMP program, often makes use of technology quite similar to that being used at lower frequencies, it is necessary to assure that the materials, transmission lines, and components all have appropriate characteristics for operation at the microwave frequencies required for the intended system applications. Therefore, Hughes has done extensive evaluation of transmission media and interconnect structures planned for use in their HDMP MCA assemblies. The resulting data provides a quantitative basis for construction of accurate component CAD models and also supports data driven choices on "best performance" implementation of such features as layer-to-layer interconnect media. Of particular interest is the approach used to interconnect the three circuit "tiles". Two methods are under consideration; the first makes use of elastomeric interconnects; the second "fuzz buttons".

Although elastomeric interconnects are less expensive, fuzz buttons offer lower loss characteristics. The three tiles are separated by aluminum ring frames which have pins to assure proper alignment of the overall structure. A kovar sleeve completes the outside of the package.

Texas Instruments is working with Martin Marietta, General Electric Central Research and Development, Lockheed, HP/EEsof and CPS to develop 2x2 module arrays based upon the General Electric/Martin Marietta developed Microwave High Density Interconnect (MHDI) approach of connecting electrical functions. In this approach, MMICs (and other components) are mounted face up in cavities that are formed in substrate layers fabricated from the metal matrix composite aluminum-silicon carbide. Aluminum-silicon carbide was selected because of its light weight, excellent thermal properties and because, by tailoring the percentage of silicon carbide in the overall mix, a nearly perfect CTE (coefficient of thermal expansion) match can be achieved with the gallium arsenide MMIC chips. Interconnections between MMICs are achieved by metal patterns embedded in multiple thin layers of polyimide material which cover the circuits. Two sets of MMICs and interconnection layers are used in the TI team approach, a transmit layer set and a control layer set. The layers are connected to each other by an elastomeric preform. Energy storage capacitors for pulsed operation are mounted below the control layer. The entire assembly is compact and if sufficient quantities are produced, should be inexpensive as well. Challenges currently being addressed by Texas Instruments and Martin Marietta include providing sufficient heat removal from the assembly to avoid device reliability problems and covering or capping MMICs with the interconnection layers without degrading microwave frequency performance. Texas Instruments will demonstrate a ninety-six element brassboard containing twenty-four 2x2 arrays, fabricated by Martin Marietta, at the conclusion of its contract in 1997.

Westinghouse is teamed with IBM, Microelectronics Center of North Carolina (MCNC), and TRW for their HDMP program. Similar to the Hughes Aircraft Company approach, Westinghouse is using MMICs and silicon digital integrated circuits mounted in a flip-chip configuration. Initially, 2x2 arrays are being fabricated; however, in the future, Westinghouse plans to extend its approach to 4x4 and 6x6 arrays to save on the cost of fabrication and array assembly. Westinghouse maintains a standard thermal path through the backside of its flip-chip MMICs for efficient heat removal. The RF sections of its modules are constructed using multiple layers of low temperature co-fired ceramic (LTCC) material and the DC or low frequency sections are constructed using multiple layers of high temperature co-fired ceramic (HTCC). The two sets of layers will be placed together in a "sandwich" using a "button board" interconnect to form the overall assembly. IBM is transferring its mature C4 technology for the flip-chip bumping of the silicon integrated control circuits to Westinghouse while MCNC is developing a variation of flip-chip bumps better suited for use with microwave circuits fabricated from gallium arsenide. TRW is producing enhanced computer aided design software to augment present MCA design capabilities.

There are four smaller efforts under way under HDMP sponsorship. The first of these, is the development of a two layer wafer coating process that will provide both hermeticity and scratch protection for the GaAs MMIC chips. If successful, these coatings will allow the possibility of using extremely low cost plastic housings for military modules rather than ones fabricated from more expensive ceramics or metal matrix composites. The materials being investigated include Benzocyclobutanes (BCB) and parylene for the layer closest to the gallium arsenide wafers with overcoatings of amorphous hydrogenated silicon carbide (a-SiC:H) or silicon nitride for the hermetic outer layer. Dow Corning and Rensselaer Polytechnic Institute are assisting M/A-COM on this program. The second effort, by Georgia Institute of Technology is directed toward development of a database of packaging material properties. It is expected that this database will be developed in a format compatible with that used by CAD vendors who are producing software for the analysis and simulation of performance of microwave and millimeter-wave MCAs. The final two programs, being carried out by Hewlett-

Packard/EEsof and Compact Software, are focused upon the development of models, analysis tools and performance simulation tools for microwave frequency packages. Because of the complexity of these packages and the circuits they house, it is necessary to develop advanced software packages that can accurately and quickly analyze mechanical and thermal properties of proposed architectures as well as their electrical properties.

CONCLUSION

In summary, although the HDMP program has limited financial resources, it is expected to result in considerable progress toward development of advanced T/R module and multi-chip assembly manufacturing procedures that are low cost but provide high quality performance. The manufacturing processes being developed are applicable to DoD phased array radar implementations as well as to a number of potential commercial applications such as transmission of entertainment to aircraft from satellite sources. In the future, programs such as the new Microwave and Analog Front End Technology (MAFET) program will augment the efforts begun under HDMP funding to provide additional computer aided design resources and to extend the development, assembly, and test of advanced MCAs to other frequency ranges and other applications.